Rejection of Claims under 35 USC §102 by Feldmeier

Claims 1, 2, 6, 7, 16, 29-32, 36, 39-40, 51, 57, 60-61, 73-74, and 85-86 are rejected under 35 USC §102(b) as anticipated by U.S. Patent No. 5,920,886 to Feldmeier. Applicants respectfully traverse these rejections, as discussed below.

Rejection of Claims under 35 USC §102 by Ross

Claims 1, 2, 6, 7, 16, 29-32, 36, 39-40, 51, 57, 60-61, 73-74, and 85-86 are alternately rejected under 35 USC §102(e) as anticipated by U.S. Patent No. 6,389,506 to Ross. Applicants respectfully traverse these rejections, as discussed below.

Rejection of Claims under 35 USC §103

Claims 3-5, 17-22, 42, 43, 49, 50, 58-59, 62-66, 69-70, and 75-79 are rejected under 35 USC §103(a) as being unpatentable over Feldmeier ('866) or Ross ('506) in view of U. S. Patent No. 6,289,414 to Feldmeier. Applicants respectfully traverse these rejections, as discussed below.

Claims 1-7, 16, and 58

Applicants' Claim 1, as amended, recites:

A content addressable memory (CAM) system including an array of binary CAM cells segmented into a plurality of array groups, each array group having a group global mask for storing a mask pattern indicating priority of the array group, wherein during compare operations between a comparand word and data stored in the array group the mask pattern masks the comparand word and is not compared with the data stored in the array group.

Neither Feldmeier ('886) nor Ross discloses or suggests the CAM device recited in Applicants' Claim 1.

Feldmeier ('886) discloses storing ternary address values in a binary CAM by breaking each ternary address value into a binary address and a corresponding priority mask. The binary address values are stored in the binary CAM, and the priority masks are stored in a separate mask list in hierarchical order (see col. 7, lines 30-45). Thus, as illustrated in Feldmeier ('886)'s FIG. 10A, each of Feldmeier ('886)'s binary address values, which are stored in rows 1030 of CAM 1020, has its own priority mask stored in a corresponding row of priority CAM 1040.

There is no language in Feldmeier ('886) that discloses or suggest a CAM array that is segmented in a plurality of array groups, as recited in Applicants' Claim 1. Further, in contrast to Applicants' Claim 1, Feldmeier ('886) teaches that each of its binary address entries has its own corresponding priority mask. Accordingly, Feldmeier ('886) also fails to disclose or suggest a group global mask that stores a mask pattern indicating priority of the array group, as recited in Applicants' Claim 1.

To anticipate a claim under 35 USC §102, each and every element of the claim must be disclosed in a single reference[1]. The exclusion of a claimed element, no matter how insubstantial or obvious, from a prior art reference is enough to negate anticipation under 35 USC §102.[2] Because Feldmeier ('886) fails to disclose or teach "an array of binary CAM cells segmented into a plurality of array groups, each array group having a group global mask for storing a mask pattern indicating priority of the array group," as recited in Applicants' Claim 1, Feldmeier ('886) neither anticipates nor renders obvious Claim 1. Accordingly, Applicants respectfully request the Examiner to withdraw the rejection of Claim 1 over Feldmeier ('886).

Ross fails to disclose or suggest a segmented CAM array in which "during compare operations between a comparand word and data stored in the array group the mask pattern masks the comparand word and is not compared with the data stored in the array group," as recited in Applicants' Claim 1. I contrast, Ross states that "for each entry 210, the input value is compared against both its entry matching value and its associated entry matching mask" (col. 4, lines 44-46). Accordingly, Ross seems to teach away[3] from Applicants' Claim 1, and therefore neither anticipates nor renders obvious Applicants' Claim 1.

Claims 2-7, 16, and 58 depend from Claim 1 and therefore distinguish over the cited references for at least the same reasons as Claim 1.

Claims 8 and 9

The Examiner indicates that Claim 8 would be allowable if re-written in independent form. In response thereto, Claim 8 has been re-written in independent form to include the

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1 Corning Glass Works v. Sumitomo Electric, 9 USPQ2d 1962, 1965 (Fed. Cir. 1989).

2 Connell v. Sears, Roebuck & Co., 220 USPQ 193, 198 (Fed. Cir. 1983).

3 In general, a reference will teach away if it suggests that the line of development flowing from the reference's disclosure is unlikely to be productive of the result sought by the applicant. In re Gurley, 27 F.3d 551, 553 (Fed. Cir. 1994).

limitations of base Claim 1, is therefore allowable over the cited references.

Claim 9 depends from Claim 8 and therefore distinguishes over the cited references for at least the same reasons as Claim 8.

Claims 10-15

The Examiner indicates that Claim 10 would be allowable if re-written in independent form. In response thereto, Claim 10 has been re-written in independent form to include the limitations of base Claim 1, is therefore allowable over the cited references.

Claims 11-15 depend from Claim 10 and therefore distinguish over the cited references for at least the same reasons as Claim 10.

Claims 17 and 21-28

Claim 21 has been re-written in independent form and, as amended, recites:

A content addressable memory (CAM) system, comprising:

an array of binary CAM cells segmented into a plurality of array groups, each array group having a group global mask for storing a mask pattern indicating priority of the array group; and

an index circuit to generate a next free address (NFA) for the data according to its priority.

None of the cited references, whether taken alone or in combination, discloses or suggests the CAM device recited in Applicants' Claim 21.

As discussed above with respect to Claim 1, Feldmeier ('886) fails to disclose or suggest "an array of binary CAM cells segmented into a plurality of array groups, each array group having a group global mask for storing a mask pattern indicating priority of the array group," as recited in Applicants' Claim 21. Feldmeier ('886) also fails to disclose or suggest "an index circuit to generate a next free address (NFA) for the data according to its priority," as recited in Claim 21. Accordingly, Claim 21 is patentable over Feldmeier ('886).

Ross fails to disclose or suggest "an index circuit to generate a next free address (NFA) for the data according to its priority," as recited in Applicants' Claim 21, nor has the Examiner pointed to any such index circuit in Ross. Accordingly, Claim 21 is patentable over Ross.

The Examiner states that Feldmeier ('414) discloses "an index circuit to generate a next free address (col. 9 lines 25-27)." Applicants disagree. The language in Feldmeier ('414) referred to by the Examiner merely summarizes a block-edge sorting method that includes "tracking (1) the first address of each of the blocks (floor); (2) the next free address of each of the blocks (nxtfree); and (3) the size of each of the blocks." Feldmeier ('414) fails to disclose or suggest any circuit or architecture that generates a next free address based upon data priority. Further, Feldmeier ('414) fails to disclose or suggest that the generation of any next free address occurs within the CAM device. Accordingly, Feldmeier ('414) fails to disclose or suggest a CAM device that includes "an index circuit to generate a next free address (NFA) for the data according to its priority," as recited in Applicants' Claim 21, nor has the Examiner pointed to any such language. Accordingly, Claim 21 is patentable over Feldmeier ('414).

Thus, because neither of the Feldmeier references nor the Ross reference disclose or suggest a CAM device that includes "an index circuit to generate a next free address (NFA) for the data according to its priority," Claim 21 is patentable over Feldmeier ('866) or Ross in view of Feldmeier ('414).

Claims 17 and 22-28 depend from Claim 21 and therefore distinguish over the cited references for at least the same reasons as Claim 21.

Claim 22 further distinguishes over the cited references because Claim 22 recites a select circuit having "a plurality of inputs to receive valid bits from the plurality of array groups" and having "a plurality of outputs to provide qualified valid bits for the plurality of array groups." The Examiner has not pointed to any language in any of the cited references that discloses or even suggests a select circuit that provides qualified valid bits to the array groups, as recited in Applicants' Claim 22. Indeed, the subject matter recited in Claim 22 is similar to that recited in Claim 10, which the Examiner has indicated as being allowable over the cited references.

Claims 29-38 and 59

Applicants' Claim 29, as amended, recites:

A content addressable memory (CAM) system, comprising:

an array of binary CAM cells segmented into a plurality of array groups, each array group assigned a priority;

a plurality of group global masks, each for storing a mask pattern indicating priority of a

corresponding array group;

a priority table including a plurality of rows, each for storing the priority of a corresponding array group.

Neither Feldmeier ('886) nor Ross discloses or suggests the CAM device recited in Applicants' Claim 29.

As discussed above with respect to Claim 1, Feldmeier ('886) fails to disclose or suggest "an array of binary CAM cells segmented into a plurality of array groups, each array group assigned a priority," as recited in Applicants' Claim 29. Accordingly, Feldmeier ('886) also fails to disclose or suggest "a plurality of group global masks, each for storing a mask pattern indicating priority of a corresponding array group," as recited in Applicants' Claim 29.

Further, Feldmeier ('886) fails to disclose or suggest "a priority table including a plurality of rows, each for storing the priority of a corresponding array group," as recited in Claim 29. The Examiner seems to equate the priority table recited in Applicants' Claim 29 with Feldmeier ('886)'s priority CAM 1040. However, while each entry in the priority table recited in Applicants' Claim 29 stores a priority for a corresponding array group having multiple rows of CAM cells, each entry in Feldmeier ('886)'s priority CAM 1040 stores a priority for a single row of CAM cells. Accordingly, Applicants' Claim 29 is patentable over Feldmeier ('886).

Ross fails to disclose or suggest both "a plurality of group global masks, each for storing a mask pattern indicating priority of a corresponding array group" and "a priority table including a plurality of rows, each for storing the priority of a corresponding array group," as recited in Applicants' Claim 29. Ross is silent as to whether a separate table exists that stores priorities for corresponding array groups. Indeed, the Examiner has not pointed to any language in Ross that discloses or even suggests a "a priority table including a plurality of rows, each for storing the priority of a corresponding array group." Accordingly, Claim 29 is patentable over Ross.

Claims 30-38 and 59 depend from Claim 29 and therefore distinguish over the cited references for at least the same reasons as Claim 29.

Claims 39-40 and 42-57

Applicants' Claim 39, as amended, recites:

A method of operating a content addressable memory (CAM) system including an array of binary CAM cells segmented into a plurality of array groups, comprising:

assigning a priority to one or more array groups; and

selectively storing data in the array groups according to priority, wherein assigning the priority comprises:

for each array group, storing a mask pattern indicative of the priority assigned to the array group in a global mask for the binary array group; and

during compare operations between a comparand word and data stored in the array groups, masking the comparand word with corresponding mask patterns without comparing the mask patterns to the data stored in the corresponding array group.

Neither Feldmeier ('886) nor Ross discloses or suggests the CAM device recited in Applicants' Claim 39.

As discussed above with respect to Claim 1, Feldmeier ('886) fails to disclose or suggest an array of binary CAM cells segmented into a plurality of array groups, with each array group having a group global mask for storing a mask pattern indicating priority of the corresponding array group. Accordingly, Feldmeier ('886) also fails to disclose or suggest "assigning a priority to one or more array groups" or "selectively storing data in the array groups according to priority," as recited in Applicants' Claim 39. Therefore, Claim 39 is patentable over Feldmeier ('886).

As discussed above with respect to Claim 1, Ross teaches that "for each entry 210, the input value is compared against both its entry matching value and its associated entry matching mask" (col. 4, lines 44-46). Accordingly, because Ross seems to teach away from Applicants' Claim 39, Claim 39 is patentable over Ross.

Claims 40 and 42-57 depend from Claim 39 and therefore distinguish over the cited references for at least the same reasons as Claim 39.

Claims 60-62 and 64-72

Claim 60, as amended, recites:

A content addressable memory (CAM) comprising:

a plurality of CAM array groups each including a plurality of rows of binary CAM cells;

a plurality of group global mask circuits each coupled to a corresponding one of the CAM array groups, wherein each group global mask indicates a priority of the corresponding group of CAM cells relative to other CAM array groups; and

a plurality of mask valid bits, each indicating whether a valid global mask is stored in a corresponding group global mask circuit.

None of the cited references, whether taken alone or in combination, discloses or suggests the CAM device recited in Applicants' Claim 60.

As discussed above with respect to Claim 1, Feldmeier ('886) fails to disclose or suggest "a plurality of CAM array groups each including a plurality of rows of binary CAM cells" and "a plurality of group global mask circuits each coupled to a corresponding one of the CAM array groups," as recited in Claim 60. Feldmeier ('886) also fails to disclose or suggest "a plurality of mask valid bits, each indicating whether a valid global mask is stored in a corresponding group global mask circuit," as recited in Claim 60. Therefore, Claim 60 is patentable over Feldmeier ('886).

Ross fails to disclose or suggest "a plurality of mask valid bits, each indicating whether a valid global mask is stored in a corresponding group global mask circuit," as recited in Applicants' Claim 60, nor has the Examiner pointed to any such language in Ross. Accordingly, Claim 60 is patentable over Ross.

The Examiner states that Feldmeier ('414) "further discloses valid bits (col. 2 lines 53-57)." The language in Feldmeier ('414) referred to by the Examiner describes valid bits for rows of a CAM array, not mask valid bits for the group global mask circuits that store mask patterns for corresponding array groups. Indeed, as discussed in Applicants' earlier response to the Office Action dated January 21, 2003, Feldmeier ('414) fails to disclose or suggest a CAM having a plurality of array groups and a plurality of group global mask circuits that store mask patterns indicating the groups' priorities.[4] Therefore, Feldmeier ('414) also fails to disclose or suggest "a plurality of mask valid bits, each indicating whether a valid global mask is stored in a corresponding group global mask circuit," as recited in Applicants' Claim 60. Accordingly, Claim 60 is patentable over Feldmeier ('414).

Because none of the cited references disclose or suggest "a plurality of mask valid bits, each indicating whether a valid global mask is stored in a corresponding group global mask

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4 See page 20 of Applicants' response of April 21, 2003.

circuit," Applicants' Claim 60 is not obvious over Feldmeier ('886) or Ross in view of Feldmeier ('414). Therefore, Applicants respectfully request the Examiner to withdraw the rejection of Claim 60.

The amendment to Claim 60 incorporates subject matter originally recited in Claim 62, and therefore does not necessitate a new search.

Claims 61-62 and 64-72 depend from Claim 60 and therefore distinguish over the cited references for at least the same reasons as Claim 60.

Claims 73-84

Claim 73 recites:

A content addressable memory (CAM) comprising:

a plurality of CAM array groups each including a plurality of rows of binary CAM cells; and

means for assigning a first priority to a first and a second of the CAM array groups, and for assigning a second priority to a third of the CAM array groups, wherein the first and second priorities are different, and wherein the third CAM array group occupies an address space numerically between address spaces occupied by the first and second CAM array groups.

As discussed above with respect to Claim 1, Feldmeier ('886) fails to disclose or suggest "a plurality of CAM array groups each including a plurality of rows of binary CAM cells," as recited in Applicants' Claim 73. Further, Feldmeier ('886) also fails to disclose or suggest "means for assigning a first priority to a first and a second of the CAM array groups, and for assigning a second priority to a third of the CAM array groups, wherein the first and second priorities are different, and wherein the third CAM array group occupies an address space numerically between address spaces occupied by the first and second CAM array groups," as recited in Claim 73. Indeed, Feldmeier ('886) teaches that his list of mask values are "sorted in hierarchical order"[5], and therefore seems to teach away from Applicants' Claim 73. Accordingly, Claim 73 is patentable over Feldmeier ('886).

There is no language in Ross disclosing or suggesting that priorities can be assigned to CAM blocks in an out-of-order or random fashion, nor has the Examiner pointed to any such language in Ross. Accordingly, because Ross fails to disclose or suggest "means for assigning a first priority to a first and a second of the CAM array groups, and for assigning a second priority

to a third of the CAM array groups, wherein the first and second priorities are different, and wherein the third CAM array group occupies an address space numerically between address spaces occupied by the first and second CAM array groups," Claim 73 is patentable over Ross.

Claims 74-84 depend from Claim 73, and therefore distinguish over the cited references for at least the same reasons as Claim 73.

New Claims 89-98

Applicants' Claim 89 recites:

A content addressable memory (CAM) device, comprising:

a plurality of CAM array groups, each array group including a plurality of rows of CAM cells and a mask valid bit indicating whether the array group is assigned a priority relative to other array groups; and

an index circuit configured to generate a next free address (NFA) in response to the mask valid bits.

None of the cited references, whether taken alone or in combination, discloses or suggests the CAM device of Applicants' Claim 89.

As discussed above with respect to Claim 60, none of the cited references disclose or suggest a mask valid bit, and therefore also fail to disclose or suggest "a mask valid bit indicating whether the array group is assigned a priority relative to other array groups," as recited in Applicants' Claim 89. Further, none of the cited references disclose or suggest "an index circuit configured to generate a next free address (NFA) in response to the mask valid bits," as recited in Claim 89, nor has the Examiner pointed to any such language in the art. Accordingly, Claim 89 is patentable over the cited references.

Claims 90-98 depend from Claim 89, and therefore distinguish over the cited references for at least the same reasons as Claim 89.

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5 See col. 7, lines 39-40.

New Claims 99-100

Applicants' Claim 99 recites:

A method for providing a next free address (NFA) for a content addressable memory (CAM) having a number of array groups, each array group including a plurality of rows of CAM cells, comprising:

providing a number of mask valid bits, each indicating whether a corresponding array group is assigned a priority; and

generating the NFA in response to the mask valid bits.

None of the cited references, whether taken alone or in combination, discloses or suggests the CAM device of Applicants' Claim 99.

As discussed above with respect to Claim 89, none of the cited references disclose or suggest a mask valid bit indicating whether a corresponding array group is assigned a priority, and none of the cited references disclose or suggest an index circuit that generates a next free address in response to the mask valid bits. Accordingly, none of the cited references disclose or suggest "providing a number of mask valid bits, each indicating whether a corresponding array group is assigned a priority" or "generating the NFA in response to the mask valid bits," as recited in Applicants' Claim 89. Thus, Claim 89 is patentable over the cited references.

Claim 100 depends from Claim 98, and therefore distinguishes over the cited references for at least the same reasons as Claim 99.

CONCLUSION

In light of the above amendments and remarks, it is believed that Claims 11-40, 42-62, 64-84, and 89-100 are in condition for allowance and, therefore, a Notice of Allowance of Claims 1-40, 42-62, 64-84, and 89-100 is respectfully requested. If the Examiner's next action is other than allowance as requested, the Examiner is requested to call the undersigned at (415) 291-9497.

Respectfully submitted,

Dated: July 12, 2004

William L Paradice III
Reg. No. 38,990

CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, Arlington, VA 22313 on July 12, 2004.

By: _____
William L Paradice III